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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,217	03/29/2001	Ha Zoong Kim	0465-0751P-SP	2187

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EXAMINER

GUERRERO, MARIA F

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 06/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/820,217

Applicant(s)

KIM, HA ZOONG

Examiner

Maria Guerrero

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 23 May 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) 1-4 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 5-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

1. This Office Action is in response to the Preliminary amendment filed March 29, 2001 and the Election filed May 23, 2002.

Claims 1-12 are pending.

### *Election/Restrictions*

2. Applicant's election with traverse of Group II claims 5-12 in Paper No. 7 is acknowledged. The traversal is on the ground(s) that no serious burden is presented to the Examiner to consider all of the claims in a single application. This is not found persuasive because the "assumption" that a close relationship exists between the two inventions is apparent, however this in itself does not overcome the restriction requirement. According to M.P.E.P. § 803, the proper criteria between for a restriction is (1) the inventions must be independent and separate and (2) there must be a serious burden on the Examiner if the restriction is not required. The product and the process of manufacturing a semiconductor device are considered to be a separate and independent by the Office. They are classified in two different art classifications and assigned to two different sets of Art Units. The examination of two independent inventions is considered to be a serious burden on the Examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claims 1-4 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

***Claim Objections***

3. Claims 7-8 are objected to because of the following informalities: claims 7-8 recite "the semiconductor device of claim 5". The independent claim 5 recites "a method of manufacturing a semiconductor device". Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

4. Claims 5-7, 9-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirabayashi (U.S. 5,614,445).

Hirabayashi teaches preparing a semiconductor substrate of a first conductivity type, forming scribe lanes in the semiconductor substrate to define chip formation areas, and forming a deep well area in each chip formation area (Fig. 1-4, 6-12, col. 4, lines 40-60). Hirabayashi discloses the deep well area having a second conductivity type opposite the first conductivity type, and forming at least one well area within the deep well area (col. 5, lines 10-25, col. 6, lines 5-25). Hirabayashi shows the first

conductivity type being P-type and the second conductivity type being N-type (Fig. 3-4, 11-12). In addition, Hirabayashi teaches the use of the plasma processing (col. 4, lines 65-67).

5. Claims 5 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (U.S. 6,159,826).

Kim et al. teaches preparing a semiconductor substrate of a first conductivity type, forming scribe lanes in the semiconductor substrate to define chip formation areas, and forming a deep well area in each chip formation area (Fig. 3-5, col. 3, lines 5-25). Kim et al. discloses the deep well area having a second conductivity type opposite the first conductivity type, and forming at least one well area within the deep well area (Fig. 8, col. 3, lines 25-32). Kim et al. shows the first conductivity type being N-type and the second conductivity type being P-type (col. 3, lines 30-35).

### ***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Fukada et al. (JP06-005583) teaches preparing a semiconductor substrate of a first conductivity type, forming scribe lanes in the semiconductor substrate to define chip formation areas, and forming a deep well area in each chip formation area.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 703-305-0162.


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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MG  
MG

June 14, 2002

  
CARL WHITEHEAD, JR.  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800